

## KVR1066D3E7/1G 1GB 128M x 72-Bit PC3-8500 CL7 ECC 240-Pin DIMM

### DESCRIPTION:

This document describes ValueRAM's 128M x 72-bit 1GB (1024MB) DDR3-1066 CL7 SDRAM (Synchronous DRAM) ECC memory module, based on eighteen 64M x 8-bit DDR3-1066 FBGA components. The SPD is programmed to JEDEC standard latency 1066Mhz timing of 7-7-7 at 1.5V. This 240-pin DIMM uses gold contact fingers and requires +1.5V. The electrical and mechanical specifications are as follows:

### FEATURES:

- JEDEC standard 1.5V ± 0.075V Power Supply
- VDDQ = 1.5V ± 0.075V
- 533MHz fCK for 1066Mb/sec/pin
- 8 independent internal bank
- Programmable CAS Latency: 5,6,7,8,9,10
- Posted CAS
- Programmable Additive Latency: 0, CL - 2, or CL - 1 clock
- Programmable CAS Write Latency(CWL) = 7(DDR3-1066)
- 8-bit pre-fetch
- Burst Length: 8 (Interleave without any limit, sequential with starting address "000" only), 4 with tCCD = 4 which does not allow seamless read or write [either on the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- Internal(self) calibration : Internal self calibration through ZQ pin (RZQ : 240 ohm ± 1%)
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower than TCASE 85°C, 3.9us at 85°C < TCASE . 95°C
- Asynchronous Reset
- 1066Mbps CL7 doesn't have backward compatibility with 800Mbps CL5
- PCB : Height 1.180" (30.00mm), double sided component

### PERFORMANCE:

<input checked="" type="checkbox"/> CL(IDD)	7 cycles
<input checked="" type="checkbox"/> Row Cycle Time (tRCmin)	50.63ns (min.)
<input checked="" type="checkbox"/> Refresh to Active/Refresh Command Time (tRFCmin)	90ns
<input checked="" type="checkbox"/> Row Active Time (tRASmin)	37.5ns (min.)
<input checked="" type="checkbox"/> Power	TBD W (operating)
<input checked="" type="checkbox"/> UL Rating	94 V - 0
<input checked="" type="checkbox"/> Operating Temperature	0° C to 85° C
<input checked="" type="checkbox"/> Storage Temperature	-55° C to +100° C

**MODULE DIMENSIONS:**